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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/726,220	11/28/2000	Farhad Fouladi	723-974	7835

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NIXON & VANDERHYE, P.C.
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 09/726,220	**Applicant(s)** FOULADI ET AL.	
	Examiner Joni Hsu	**Art Unit** 2628	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 15 March 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: _____.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: see attached sheets.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

Applicant argues that the 3/22/2006 Office Action does not set forth a proper basis for the rejections of Claims 16, 27 and 40 because it fails to address the specific limitations present in the claims, and a discussion of the specific limitations of Claims 16, 27 and 40 is presented for the first time in 12/15/2006 Office Action and therefore the 12/15/2006 Office Action should not have been made final (page 12).

In reply, the Examiner disagrees. In the 3/22/2006 Office Action, Claims 16 and 27 were rejected under the same rationale as Claim 1, and Claim 40 was rejected under the same rationale as Claim 14. In the 12/15/2006 Office Action, the rejections for these claims were explicitly written out, however the same citations were used for Claims 16 and 27 as were used in Claim 1, and the same citations were used for Claim 40 as was used in Claim 14. Therefore, since these citations were previously presented in the 3/22/2006 Office Action, the 12/15/2006 Office Action could be made final.

Applicant argues that Applicants' own disclosure cannot be used to re-characterize the disclosure of an applied reference so that this disclosure can thereby be used to reject claims (page 13).

In reply, the Examiner points out that the Applicants' own disclosure was merely used to define what is meant by Applicants' claimed "memory controller". Since Applicants' own disclosure defines the claimed "memory controller" in the same manner as the "interface controller" of Chin (US006202101B1), the "interface controller" of Chin is considered to be equivalent to the claimed "memory controller".

Applicant argues that Figure 8 is a non-limiting example embodiment and the claims are not limited to this specific embodiment (page 13).

In reply, the Examiner points out that Figure 8 appears to be the only detailed block diagram of the memory controller described in the disclosure, and there does not appear to be any detailed description of any other memory controller embodiments in the disclosure. Since the description of Figure 8 appears to be the only detailed description of the memory controller in the disclosure, the memory controller of Figure 8 is considered to be the claimed memory controller.

Applicant argues that an assertion that the entirety of the interface controller 14 of Chin can be viewed as a memory controller is simply a contrivance to remedy Chin's manifest failure to disclose that queue 68 is part of a memory controller 44 (page 13).

In reply, the Examiner points out that since Applicants' disclosure defines the claimed "memory controller" in the same manner as the "interface controller" of Chin, the "interface controller" of Chin is considered to be equivalent to the claimed "memory controller".

Applicant argues that in Chin, while the requests in queue 68 from the processor bus might be sent to different destinations, the requests are from a single resource and there is no disclosure in Chin that queue 68 is a multiple resource buffer for storing requests for main memory access from each of a plurality of resources (page 14).

In reply, the Examiner points out that Chin discloses that "the processor bus can link at least one, and certainly more, processors" (Col. 3, lines 17-19). Since the processor bus links a plurality of processors, and queue 68 receives requests from the processor bus (Col. 12, lines 44-47), queue 68 receives requests from a plurality of processors, and therefore queue 68 is a

multiple resource buffer for storing requests for main memory access from each of a plurality of resources.

Applicant argues that queue 50c of Chin is not involved with a transfer of information from buffer memories to a multiple resource buffer (page 14).

In reply, the Examiner points out that multiple resource buffer 68 receives memory requests from the processor bus (Col. 12, lines 44-47). The memory request will access a memory location and data at that location is temporarily stored within an M2P queue 50c (Col. 12, lines 65-67). M2P queue 50c is connected between the memory 18 and processor 12, and therefore M2P queue 50c is connected to the processor bus. Therefore, queue 50c is involved with a transfer of information from buffer memories to a multiple resource buffer 68.

Applicant argues that queue 50c stores data read from the memory after a memory request is processed, and therefore queue 50c is not a request queue (page 15).

In reply, the Examiner points out that Chin discloses that a bus interface unit dispatches memory request cycles to respective target devices (Col. 1, lines 10-15). Figure 2 is a diagram of the bus interface unit (Col. 6, lines 50-54), and shows that cycles are passed between controllers using queues which link respective controllers (Col. 8, lines 23-44). Since cycles are passed using the queues, and these cycles are memory request cycles, the queues are considered to store information indicative of a request for main memory access, as recited in Claim 1.

Applicant argues that Chin describes queues that involve requests from the processor bus, not from a plurality of buffer memories each of which is operatively coupled to one of a plurality of resources requesting memory access (page 15).

In reply, the Examiner points out that the processor bus is linked to a plurality of processors (Col. 3, lines 17-19). Since the queues involve requests from the processor bus, the queues involve requests from a plurality of resources. These requests include requests for accessing memory (Col. 8, lines 20-37). Therefore Chin discloses that the queues are a plurality of buffer memories each of which is operatively coupled to one of a plurality of resources requesting memory access.

Applicant argues that Chin discloses de-queuing for queue 50c, which contains data whose source is the memory and whose destination is the processor. This queue is not a write request queue and there is no disclosure in Chin of initiating the flushing of a resource's write request queue when that resource is writing to main memory (page 16). The last few lines of this disclosure state: "If the memory request is a write request, then the address will be held in the P2M queue (queue 50a) until that request's entry number matches the current in-order queue entry number." This description relates to write requests, but simply describes how long an address is held in a queue. There is nothing about the flushing of a write request (page 18).

In reply, the Examiner points out that Chin describes, "Arranging the order in which data is de-queued from queue 50c depends on where the pointer is relative to queue 64. For example, if pointer 76 is at entry numeral 0, then data is not de-queued from queue 50c until pointer arrives at entry number 1, in the example shown. Once pointer 76 is at entry number 1, then data attributed to entry numeral 1 is de-queued and thereafter presented to the processor bus. If the memory request is a write request, then the address will be held in P2M queue (queue 50a) until that request's entry number matches the current in-order queue entry number" (Col. 13, lines 1-

11). Since this describes how long an address is held in a queue, it also teaches that the address will eventually not be held in a queue any longer, and therefore will be de-queued. Therefore, for the case of the write request queue, once that request's entry number matches the current in-order queue entry number, then the data attributed to that entry number is de-queued. Therefore, Chin does disclose initiating the flushing of a resource's write request queue when that resource is writing to main memory.

Applicant argues that the office action provides no explanation as to how the "grouping" of read and writes to reduce turn around time as disclosed in Harriman (US006092158A) is similar to the claimed delaying (page 17).

In reply, the Examiner points out that Harriman discloses grouping reads and writes to reduce bus turn around, and reducing bus turn around means reducing the frequency of switching between memory read states and memory write states. Since the reads are grouped together and the writes are grouped together, this means that if the bus is currently in the memory read state, the forwarding of requests for main memory write access to a memory control circuit are delayed since only read requests are being forwarded since reads are grouped together.

Applicant argues that queues 50d and 50h are a memory-to-PCI queue and a memory-to-AGP queue, respectively, and store data read from the memory, not requests for such data (page 17).

In reply, the Examiner points out that Chin discloses that a bus interface unit dispatches memory request cycles to respective target devices (Col. 1, lines 10-15). Figure 2 is a diagram of the bus interface unit (Col. 6, lines 50-54), and shows that cycles are passed between controllers

using queues which link respective controllers (Col. 8, lines 23-44). Since cycles are passed using the queues, and these cycles are memory request cycles, the queues are considered to store requests for main memory access, as recited in Claim 27.

KEE M. TUNG
SUPERVISORY PATENT EXAMINER